UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,835	10/08/2004	Ta-Jung Su	13129-US-PA	5834

31561 7590 09/11/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2813	

NOTIFICATION DATE	DELIVERY MODE
09/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

TH

Office Action Summary	Application No.	Applicant(s)	
	10/711,835	SU ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,11-13 and 17-18* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7,11-13 and 17-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/15/07 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Sun et al. (U.S. Patent No. 2004/0253815) in view of Yu-Chou et al. (U.S. Patent Publication No. 2004/0259294).

Referring to figures 2, Sun et al. teach method of fabricating a gate, comprising the steps of:

providing a substrate (110, see figure 1a, glass substrate);

forming a patterned mask layer (120, photoresist) over the substrate (110, see figure 2), wherein the patterned mask layer (120)exposes an area on the substrate (110) for forming the gate (see figure 2, paragraph# 11, claim 12);

forming a metallic layer (130) over the mask layer (120) and inside the exposed area such that the metallic layer (130) formed over the mask layer (120) is apart from the metallic layer(130) formed inside the exposed area (see figure 2, paragraph# 16).

Forming an oxidation-resistant layer (140/150) on the metallic layer (130), wherein the oxidation-resistant layer (140/150) formed over the mask layer (120) is apart from the oxidation-resistant layer formed inside the exposed area (see figure 2, paragraph# 16); and

removing the mask layer (see figure 2, paragraph# 16), wherein the metallic layer and the oxidation-resistant layer formed over the mask layer is removed at the same time and the metallic layer and the oxidation-resistant layer formed inside the exposed area is remained so as to form the gate (see claim 12).

Regarding to claims 5, 11, 17, wherein the step of forming the gate comprises performing a physical vapor deposition process (sputtering technique is PVD, see paragraph# 16, claim 5).

Regarding to claim 6, 12, 18, wherein the mask layer comprises a photoresist layer (120, see paragraph# 16).

However, the reference does not teach forming oxidation-resistant layer is metal silicide compound.

Yu-Chou et al. teaches forming a first metal layer Al (20) on the substrate (20), forming a second metal layer (30, metal or metal silicide, see paragraph# 20, figures 2-3).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a second metal layer silicide in process of Sun et al. as taught by Y-Chou et al. because forming a metal silicide film would reduce contact impedance of a thin film transistor.

Claims 7, 11-13, 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al. (U.S. Patent No. 2004/0253815) in view of Yu-Chou et al. (U.S. Patent Publication No. 2004/0259294) in view of Lee et al. (U.S. Patent Publication No. 2006/0163582).

Referring to figures 2, Sun et al. teach method of fabricating a gate, comprising the steps of:

providing a substrate (110, see figure 1a, glass substrate);

forming a patterned mask layer (120, photoresist) over the substrate (110, see figure 2), wherein the patterned mask layer (120)exposes an area on the substrate (110) for forming the gate (see figure 2, paragraph# 11, claim 12);

forming a metallic layer (130) over the mask layer (120) and inside the exposed area such that the metallic layer (130) formed over the mask layer (120) is apart from the metallic layer(130) formed inside the exposed area (see figure 2, paragraph# 16).

Forming an oxidation-resistant layer (140/150) on the metallic layer (130), wherein the oxidation-resistant layer (140/150) formed over the mask layer (120) is apart from the oxidation-resistant layer formed inside the exposed area (see figure 2, paragraph# 16); and

removing the mask layer ((see figure 2, paragraph# 16), wherein the metallic layer and the oxidation-resistant layer formed over the mask layer are removed at the same time and the metallic layer and the oxidation-resistant layer formed inside the exposed area is remained so as to form the gate (see claim 12),

forming an insulating layer (160, see paragraph# 16) over the gate (130/140/150).

Regarding to claims 5, 11, 17, wherein the step of forming the gate comprises performing a physical vapor deposition process (sputtering technique is PVD, see paragraph# 16, claim 5).

Regarding to claim 6, 12, 18, wherein the mask layer comprises a photoresist layer (120, see paragraph# 16).

However, the reference does not teach the step of forming oxidation-resistant layer is metal silicide compound, forming a channel layer over the insulating layer above the gate, forming a source and a drain over the channel layer, and forming a passivation layer over the substrate, wherein the passivation layer has an opening that exposes a portion of the drain; and forming a pixel electrode over the passivation layer such that the pixel electrode is electrically connected to the drain via the opening. Nevertheless, the process is known in fabricating a thin film transistor as evidenced by Lee et al..

Yu-Chou et al. teaches forming a first metal layer Al (20) on the substrate (20), forming a second metal layer (30, metal or metal silicide, see paragraph# 20, figures 2-3).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a second metal layer silicide in process of Sun et al. as taught by Y-Chou et al. because forming a metal silicide film would reduce contact impedance of a thin film transistor.

Referring to figures 5a-5b, 10-12, 15a-15c, Lee et al. teaches the step of forming a TFT device comprising the steps of: forming a channel layer (see paragraph# 111), over the insulating layer (30) above the gate (26), forming a source (65) and a drain (66) over the channel layer (see paragraph# 111), and forming a passivation layer (70) over the substrate, wherein the passivation layer (70) has an opening (76) that exposes a portion of the drain (66, see figure 5a); and forming a pixel electrode (82, see figure 5a) over the passivation layer (70) such that the pixel electrode (82) is electrically connected to the drain (66) via the opening (70, see figure 5b).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would the step of forming the oxidation-resistant layer is selected from a group consisting of an alloy of metals and a metal silicide compound after forming the metallic layer, and forming a passivation layer over the substrate, wherein the passivation layer has an opening that exposes a portion of the drain; and forming a pixel electrode over the passivation layer such that the pixel electrode is electrically connected to the drain via the opening in process of Sun et al. in process of Lee et al. because the process is known the semiconductor art to fabricating a thin film transistor to provide superior adhesion ability to the substrate and diffusion resistance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN